## REMARKS

Claims 1-14 are pending in the application. In the Office Action of July 30, 2003, the Examiner made the following disposition:

- A.) Rejected claims 1-4 and 7-14 under 35 U.S.C. §103(a) as being unpatentable over *Utagawa et al.* and further in view of *Numazaki et al.*
- B.) Rejected claims 5-9 under 35 U.S.C. §112, second paragraph.

  Applicant respectfully traverses the rejections and addresses the Examiner's disposition below.
- A.) Rejection of claims 1-4 and 7-14 under 35 U.S.C. §103(a) as being unpatentable over

  Utagawa et al. and further in view of Numazaki et al.:

Applicant respectfully disagrees with the rejection.

Applicant's independent claims 1 and 14, each as amended, each claim dividing both a first light amount corresponding to a predetermined bit and a second light amount corresponding to a bit in a lower order by one bit to the bit of a video image. The first and second light amounts are divided so that a difference between division numbers of the first and second light amounts of adjacent bits whose light amounts are divided is one of 0 and 1, including a case wherein at least one of the division numbers is greater than 2.

Referring to Applicant's Figure 28A as an illustrative example, bits B0-B7 are divided by a division number. As shown, for example, bit B6 is divided 4 times, bit B5 is divided 3 times, bit B4 is divided 3 times, and bit B3 is divided 2 times. Thus, adjacent bits (e.g., bits B6 and B5) are divided so that a difference between the difference numbers is 0 or 1. In the example, the difference in the number of divisions between adjacent bits B6 (4 divisions) and B5 (3 divisions) is 1. Thus, this is the case even when one of the adjacent bits is divided by more than two divisions.

Accordingly, it is possible to distribute the divisional light amounts obtained by dividing the light amount of a bit plane of a high order (e.g., 4) in positions near divisional light amounts obtained by dividing the light amount of the bit plane of a lower order (e.g., 1). In other words, in the example of Figure 28A, the bits B0-B7 are divided into a maximum of 4 divisions, so that when the divisions are distributed (as shown in Figure 28B), a division of bit (e.g., B7) can be positioned near divisions of other bits (e.g., B6 and B4) instead of having to be positioned next to another division of the same bit (e.g., B7). Thus, if bit B7 was divided 8 times, some of the divisions of bit B7 may need to be positioned next to each other. When the divisions of the same bit are positioned next to each other, that disadvantageously results in moving picture pseudo

contours. Therefore, claims 1 and 14 beneficially avoid moving picture pseudo contours by claiming the difference value between adjacent bits to 0 or 1, including for higher order divisions of greater than 2. (See Specification, page 51, line 10 - page 53, line 17).

This is clearly unlike *Utagawa* in view of *Numazaki*. Unlike Applicant's claims 1 and 14, *Utagawa* relates to still pictures and not to video images. As described above, Applicant's claims 1 and 14 overcome the problem of moving picture pseudo contours that typically occur when a video image moves across a screen. Thus, one having skill in the art would not combine *Utagawa* with another reference to disclose or suggest Applicant's claims that correct a problem associated with video images.

The Examiner combines *Utagawa* with *Numazaki* to allegedly disclose or suggest that *Utagawa's* method could teach a specific difference in difference values. However, the combined references still fail to disclose or suggest claims 1 and 14. As stated above, *Utagawa* fails to even relate to video images, and therefore it would not have been obvious to combine *Utagawa* with another reference to address a problem associated with video images.

Further, *Numazaki* still fails to disclose or suggest Applicant's claimed division of light amounts for adjacent bits. Applicant's claims 1 and 14 beneficially divide light amounts of a signal by a division number so that a difference in division numbers of the light amounts of the adjacent bits is 0 or 1, including for a case wherein at least one of the division numbers is greater than 2. Thus, a bit of a light amount that is divided 4 times can be adjacent a bit of a light amount that is divided 3 times. This is clearly unlike *Numazaki*, which fails to even relate to associating divided light amounts with a bit field. Instead, *Numazaki* relates to delivering a number of pulses to a light unit based on a state. When *Numazaki's* state is 1 then 1 light pulse is delivered to the light, when the state is 2 then 2 pulses are delivered, and when the state is 3 then 4 pulses are sent. Nowhere does *Numazaki* even discuss dividing light amounts for a bit field.

Further, *Numazaki's* number of pulses are not divided number so that a difference in pulses between states is 0 or 1, including for a case wherein at least one of the states is greater than 2. Instead, *Numazaki's* pulses <u>double</u> for the next state.

Therefore, *Utagawa* in view of *Numazaki* fails to disclose or suggest Applicant's claims 1 and 14.

Claims 2-4 and 7-13 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Applicant respectfully submits the rejection has been overcome and requests that it be withdrawn.

## B.) Rejection of claims 5-9 under 35 U.S.C. §112, second paragraph:

Claims 5, 7, 8 and 9 have been amended as per the Examiner's request to overcome the rejection.

Claim 6 has been canceled.

Applicant respectfully submits the rejection has been overcome and requests that it be withdrawn.

## **CONCLUSION**

In view of the foregoing, it is submitted that claims 1-5 and 7-14 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

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## **CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited as First Class Mail in an envelope addressed to Commissioner for Patents, PO Box 1450, Alexandria, Virginia 22313-1450 on October 29, 2003.

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